CLAIMS

1. A method of manufacturing a semiconductor device having a nonvolatile memory cell including first and second field effect transistors which are adjacent to each other, comprising the steps of:

(a) forming a first semiconductor region of a first conduction type of said first field effect transistor by doping a main surface of a semiconductor substrate with first impurity;

(b) forming a first gate electrode of said first field effect transistor over said first semiconductor region;

(c) forming an insulating film over side surfaces of said first gate electrode;

(d) removing a part of the semiconductor substrate in a region adjacent to said first gate electrode and the insulating film by etching;

(e) forming a second semiconductor region of a second conduction type which is opposite to the first conduction type of said second field effect transistor, in a region which is said adjacent region and in which a part of the semiconductor substrate is removed by said etching, by doping the main surface of the semiconductor substrate subjected to said step (d) with second impurity; and

(f) forming a second gate electrode of said second field effect transistor over said second semiconductor region.

2. A method of manufacturing a semiconductor device

having a nonvolatile memory cell including first and second field effect transistors which are adjacent to each other, comprising the steps of:

(a) forming a first semiconductor region of a first conduction type of said first field effect transistor by doping a main surface of a semiconductor substrate with first impurity;

(b) forming a first gate electrode of said first field effect transistor over said first semiconductor region;

(c) forming an insulating film over side surfaces of said first gate electrode;

(d) forming a spacer over a side surface of said insulating film at a side over which said second field effect transistor is disposed;

(e) forming a second semiconductor region of a second conduction type which is opposite to the first conduction type of said second field effect transistor so that an end portion of said second semiconductor region at a side of a formation region of said second field effect transistor is disposed in a position apart from the side surface of said insulating film at the side of the formation region of said second field effect transistor by an amount of a thickness of said spacer by doping the main surface of said semiconductor substrate with second impurity in a state where said spacer is formed;

(f) after said step (e), removing said spacer; and

(g) after said step (f), forming a second gate electrode

of said second field effect transistor over said second semiconductor region.

3. The method of manufacturing a semiconductor device according to claim 1 or 2,

wherein said first semiconductor region is a region for forming a channel of said first field effect transistor, and

wherein said second semiconductor region is a region for forming a channel of said second field effect transistor.

4. A method of manufacturing a semiconductor device having a nonvolatile memory cell including first and second field effect transistors which are adjacent to each other, comprising the steps of:

(a) forming a first gate electrode of said first field effect transistor over a main surface of a semiconductor substrate;

(b) forming an insulating film for protection over the main surface of the semiconductor substrate around said first gate electrode;

(c) after formation of said insulating film for protection, depositing a conductive film for forming a second gate electrode of said second field effect transistor over the main surface of said semiconductor substrate;

(d) forming said second gate electrode by patterning said conductive film; and

(e) removing said conductive film remained after said step (d) by etching.

5. The method of manufacturing a semiconductor device according to claim 4,

wherein said insulating film for protection is simultaneously formed in a step of forming a gate insulating film of another field effect transistor over said semiconductor substrate.

6. The method of manufacturing a semiconductor device according to claim 4,

wherein the step of forming said insulating film for protection includes the steps of:

depositing said insulating film for protection over the main surface of said semiconductor substrate; and

patterning the deposited insulating film for protection so as to remain over the semiconductor substrate over one side surface of said first gate electrode.

7. The method of manufacturing a semiconductor device according to claim 6,

wherein the step of patterning said insulating film for protection includes the steps of:

removing also said insulating film for protection deposited over a region of connection to an upper wiring layer over a top surface of said first gate electrode; and,

forming, after the step of forming said second gate electrode, a silicide layer simultaneously over a top surface of said second gate electrode and the connection region to which said upper wiring is connected of said first gate electrode.

8. The method of manufacturing a semiconductor device according to claim 1, 2, or 4,

wherein one said first and said second field effect transistor is a field effect transistor for a memory and the other field effect transistor is a field effect transistor for selecting a memory cell,

the method further comprising the steps of:

forming a charge storage layer for storing charges contributing to data storage between a memory gate electrode of said field effect transistor for a memory and the semiconductor substrate; and

forming a gate insulating film between a control gate electrode of said field effect transistor for selecting a memory cell and the semiconductor substrate.

9. The method of manufacturing a semiconductor device according to claim 1, 2, or 4,

wherein one of said first and second field effect transistors is a field effect transistor for a memory and the other field effect transistor is a field effect transistor for selecting a memory cell,

the method further comprising the steps of:

forming a charge storage layer for storing charges contributing to data storage between a memory gate electrode of said field effect transistor for a memory and the semiconductor substrate; and

forming a gate insulating film between a control gate electrode of said field effect transistor for selecting a memory cell and the semiconductor substrate, and

said charge storage layer including discrete trap levels.

10. The method of manufacturing a semiconductor device according to claim 1, 2, or 4,

wherein one of said first and second field effect transistors is a field effect transistor for a memory and the other field effect transistor is a field effect transistor for selecting a memory cell,

the method further comprising the steps of:

forming a charge storage layer for storing charges contributing to data storage between a memory gate electrode of said field effect transistor for a memory and the semiconductor substrate; and

forming a gate insulating film between a control gate electrode of said field effect transistor for selecting a memory cell and the semiconductor substrate, and

said charge storage layer being comprised of silicon nitride.

11. The method of manufacturing a semiconductor device according to claim 1, 2, or 4,

wherein one of said first and second field effect transistors is a field effect transistor for a memory and the other field effect transistor is a field effect transistor for selecting a memory cell,

wherein the method further comprises a step of forming a charge storage layer for storing charges contributing to data storage between a memory gate electrode of said field effect transistor for a memory and a semiconductor substrate, and

wherein data is erased by extracting the charges in said charge storage layer to the memory gate electrode side.

12. The method of manufacturing a semiconductor device according to claim 1, 2, or 4,

wherein one of said first and second field effect transistors is a field effect transistor for a memory and the other field effect transistor is a field effect

transistor for selecting a memory cell,

the method further comprising the steps of:

forming a charge storage layer for storing charges contributing to data storage between a memory gate electrode of said field effect transistor for a memory and the semiconductor substrate;

forming a gate insulating film between a control gate electrode of said field effect transistor for selecting a memory cell and the semiconductor substrate; and

patterning said control gate electrode so that a part of said control gate electrode is provided over said memory gate electrode.

13. The method of manufacturing a semiconductor device according to claim 1, 2, or 4,

wherein one of said first and second field effect transistor is a field effect transistor for a memory and the other field effect transistor is a field effect transistor for selecting a memory cell,

the method further comprising the steps of:

forming a charge storage layer for storing charges contributing to data storage between a memory gate electrode of said field effect transistor for a memory and a semiconductor substrate;

forming a gate insulating film between a control gate electrode of said field effect transistor for

selecting a memory cell and the semiconductor substrate; and

patterning said memory gate electrode so that a part of said memory gate electrode is provided over said control gate electrode.

14. A method of manufacturing a semiconductor device having a nonvolatile memory cell including a charge storage layer for storing charges contributing to storage of data between a gate electrode and a semiconductor substrate, comprising the steps of:

(a) forming said charge storage layer over a main surface of said semiconductor substrate;

(b) depositing a conductive film for forming said gate electrode over said charge storage layer;

(c) forming said gate electrode by patterning said conductive film; and

(d) patterning said charge storage layer,

wherein in said step (d), a part of an end portion of said charge storage layer is etched so that a side surface of the end portion of said charge storage layer is apart from a side surface of the end portion of said gate electrode toward a center of said gate electrode.

15. The method of manufacturing a semiconductor device according to claim 14, wherein said charge storage layer includes discrete trap levels.

16. The method of manufacturing a semiconductor device according to claim 14, wherein said charge storage layer is made of silicon nitride.

17. The method of manufacturing a semiconductor device according to claim 14,

wherein said gate electrode is a memory gate electrode,

the method further comprising a step of forming a field effect transistor for selecting a memory cell so as to be adjacent to said memory gate electrode.

18. The method of manufacturing a semiconductor device according to claim 17, further comprising a step of patterning said control gate electrode of said field effect transistor for selecting a memory cell so that a part of the control gate electrode is provided over said memory gate electrode.

19. The method of manufacturing a semiconductor device according to claim 17, further comprising a step of patterning said memory gate electrode so that a part of said memory gate electrode is provided over a control gate electrode of said field effect transistor for selecting a memory cell.

20. The method of manufacturing a semiconductor device according to claim 14, wherein charges in said charge storage layer are extracted to said memory gate electrode side, thereby erasing data.

21. A semiconductor device having a nonvolatile memory cell including first and second field effect transistors which are adjacent to each other, comprising:

(a) a first gate electrode as a gate electrode of said first field effect transistor, which is formed over a semiconductor substrate;

(b) a first semiconductor region of a first conduction type formed in said semiconductor substrate below said first gate electrode;

(c) a second gate electrode as a gate electrode of said second field effect transistor, which is formed over said semiconductor substrate; and

(d) a second semiconductor region of a second conduction type opposite to the first conduction type formed in said semiconductor substrate below said second gate electrode,

wherein a main surface of the semiconductor substrate in which said second semiconductor region is formed is formed so as to be lower than a main surface of the semiconductor substrate in which said first semiconductor region is formed.

22. A semiconductor device having a nonvolatile memory

cell including first and second field effect transistors which are adjacent to each other, comprising:

(a) a first gate electrode as a gate electrode of said first field effect transistor, which is formed over a semiconductor substrate;

(b) a first semiconductor region of a first conduction type formed in said semiconductor substrate below said first gate electrode;

(c) a second gate electrode as a gate electrode of said second field effect transistor, which is formed over said semiconductor substrate via a gate insulating film; and

(d) a second semiconductor region of a second conduction type opposite to the first conduction type formed in said semiconductor substrate below said second gate electrode,

wherein an end portion of said second semiconductor region at the side of said second field effect transistor coincides with a position of an end portion of said second gate electrode at said first field effect transistor side and said gate insulating film or extends so as to be partly below a region of said second gate electrode and said gate insulating film.

23. The semiconductor device according to claim 21 or 22,

wherein said first field effect transistor is a field effect transistor for a memory, said first semiconductor region is a region for forming a channel of said field

effect transistor for a memory, and a charge storage layer for storing charges contributing to data storage is formed between a first gate electrode of said field effect transistor for a memory and a semiconductor substrate, and

wherein said second field effect transistor is a field effect transistor for selecting a memory cell, and said second semiconductor region is a region for forming the channel of said field effect transistor for selecting a memory cell.

24. The semiconductor device according to claim 21 or 22,

wherein said first field effect transistor is a field effect transistor for a memory, and a charge storage layer for storing charges contributing to data storage is formed between a first gate electrode of said field effect transistor for a memory and the semiconductor substrate,

wherein said second field effect transistor is a field effect transistor for selecting a memory cell, and said first semiconductor region has functions of a region for forming the channel of said field effect transistor for a memory and semiconductor regions for a source and a drain of said field effect transistor for selecting a memory cell, and

wherein said second semiconductor region is a region for forming the channel of said field effect transistor

for selecting a memory cell.

25. The semiconductor device according to claim 21 or 22,

wherein said first field effect transistor is a field effect transistor for a memory, said first semiconductor region is a region for forming the channel of said field effect transistor for a memory, and a charge storage layer for storing charges contributing to data storage is formed between a first gate electrode of said field effect transistor for a memory and the semiconductor substrate,

wherein said second field effect transistor is a field effect transistor for selecting a memory cell, and said second semiconductor region is a region for forming the channel of said field effect transistor for selecting a memory cell, and

wherein said charge storage layer includes discrete trap levels.

26. The semiconductor device according to claim 21 or 22,

wherein said first field effect transistor is a field effect transistor for a memory, said first semiconductor region is a region for forming the channel of said field effect transistor for a memory, and a charge storage layer for storing charges contributing to data storage is formed

between a first gate electrode of said field effect transistor for a memory and a semiconductor substrate,

wherein said second field effect transistor is a field effect transistor for selecting a memory cell, and said second semiconductor region is a region for forming the channel of said field effect transistor for selecting a memory cell, and

wherein said charge storage layer is made of silicon nitride.

27. The semiconductor device according to claim 21 or 22,

wherein said first field effect transistor is a field effect transistor for a memory, said first semiconductor region is a region for forming the channel of said field effect transistor for a memory, and a charge storage layer for storing charges contributing to data storage is formed between a first gate electrode of said field effect transistor for a memory and the semiconductor substrate,

wherein said second field effect transistor is a field effect transistor for selecting a memory cell, and said second semiconductor region is a region for forming the channel of said field effect transistor for selecting a memory cell, and

wherein a second gate electrode of said field effect transistor for selecting a memory cell is provided over said first gate electrode of said field effect transistor

for a memory.

28. The semiconductor device according to claim 21 or 22,

wherein said first field effect transistor is a field effect transistor for a memory, said first semiconductor region is a region for forming the channel of said field effect transistor for a memory, and a charge storage layer for storing charges contributing to data storage is formed between a first gate electrode of said field effect transistor for a memory and the semiconductor substrate,

wherein said second field effect transistor is a field effect transistor for selecting a memory cell, and said second semiconductor region is a region for forming the channel of said field effect transistor for selecting a memory cell, and

wherein the first gate electrode of said field effect transistor for a memory is provided over said second gate electrode of said field effect transistor for selecting a memory cell.

29. A semiconductor device having a nonvolatile memory cell including a charge storage layer for storing charges contributing to data storage between a gate electrode and a semiconductor substrate,

wherein a position of a side surface at an end in a width direction of said charge storage layer coincides

with a position of a side surface at an end in a width direction of said gate electrode or is apart from the side surface at an end in the width direction of said gate electrode toward a center of said gate electrode.

30. A semiconductor device having a nonvolatile memory cell including a charge storage layer for storing charges contributing to data storage between a gate electrode and a semiconductor substrate,

wherein said charge storage layer is formed so that its whole region in plan view is included in a whole region of said gate electrode in plan view.

31. A semiconductor device having a nonvolatile memory cell including a charge storage layer for storing charges contributing to data storage between an n-type gate electrode and a semiconductor substrate,

wherein said n-type gate electrode has a first region near said charge storage layer and a second region as another region, and concentration of n-type impurity in said first region is lower than that of the n-type impurity in said second region.

32. A semiconductor device having a nonvolatile memory cell including a charge storage layer for storing charges contributing to data storage between an n-type gate electrode and a semiconductor substrate,

wherein concentration of n-type impurity in said n-type gate electrode is lower than that of the n-type impurity in a gate electrode of an n type in another field effect transistor provided over said semiconductor substrate.

33. A semiconductor device having a nonvolatile memory cell including a charge storage layer for storing charges contributing to data storage between an n-type gate electrode and a semiconductor substrate,

wherein concentration of n-type impurity in said n-type gate electrode is $1\times10^{18}/cm^3$ to $2\times10^{20}/cm^3$.

34. A semiconductor device having a nonvolatile memory cell including a charge storage layer for storing charges contributing to data storage between an n-type gate electrode and a semiconductor substrate,

wherein concentration of n-type impurity in said n-type gate electrode is $8\times10^{19}/cm^3$ to $1.5\times10^{20}/cm^3$.

35. The semiconductor device according to claim 29, 30, 31, 32, 33, or 34,

wherein said gate electrode is a memory gate electrode, a field effect transistor for selecting a memory cell is provided so as to be adjacent to said memory gate electrode, and charges in said charge storage layer are extracted to said memory gate electrode side, thereby

erasing data.

36. A semiconductor device having a nonvolatile memory cell including a charge storage layer for storing charges contributing to data storage between an n-type gate electrode and a semiconductor substrate,

wherein electrons in said charge storage layer are extracted to said gate electrode side and positive holes in said gate electrode are injected to the charge storage layer side and promoted to recombine with said electrons, thereby erasing data.

37. A semiconductor device having a nonvolatile memory cell including a charge storage layer for storing charges contributing to data storage between a gate electrode and a semiconductor substrate,

wherein electrons in said charge storage layer are extracted to said gate electrode side, thereby erasing data, and said gate electrode is of a p type.

38. A semiconductor device having a nonvolatile memory cell in which data is erased by extracting charges stored in a charge storage layer to a gate electrode side,

wherein the lowest write level is higher than an initial threshold voltage of said nonvolatile memory cell.

39. The semiconductor device according to claim 29, 30,

31, 32, 33, 34, 36, 37, or 38, wherein said charge storage layer includes discrete trap levels.

40. The semiconductor device according to claim 29, 30, 31, 32, 33, 34, 36, 37, or 38, wherein said charge storage layer is made of silicon nitride.

41. The semiconductor device according to claim 29, 30, 31, 32, 33, 34, 36, 37, or 38, wherein said gate electrode is a memory gate electrode, and a field effect transistor for selecting a memory cell is provided so as to be adjacent to said memory gate electrode.

42. The semiconductor device according to claim 29, 30, 31, 32, 33, 34, 36, 37, or 38,

wherein said gate electrode is a memory gate electrode, a field effect transistor for selecting a memory cell is provided so as to be adjacent to said memory gate electrode, and

wherein a control gate electrode of said field effect transistor for selecting a memory cell is provided over said memory gate electrode.

43. The semiconductor device according to claim 29, 30, 31, 32, 33, 34, 36, 37, or 38,

wherein said gate electrode is a memory gate electrode, a field effect transistor for selecting a

memory cell is provided so as to be adjacent to said memory gate electrode, and

wherein said memory gate electrode is provided over a control electrode of said field effect transistor for selecting a memory cell.

44. The semiconductor device according to claim 29, 30, 31, 32, 33, 34, 36, 37, or 38,

wherein said gate electrode is a memory gate electrode, a field effect transistor for selecting a memory cell is provided so as to be adjacent to said memory gate electrode, and

wherein a first semiconductor region of a first conduction type provided in a semiconductor substrate below said memory gate electrode has a function of a region for forming a channel of a first field effect transistor for a memory having said memory gate electrode and a function of semiconductor regions for a source and a drain of said field effect transistor for selecting a memory cell.

45. The semiconductor device according to claim 29, 30, 31, 32, 33, 34, 36, 37, or 38,

wherein a width of said gate electrode in a width direction of said gate electrode is larger than or equal to a width of said charge storage layer in the width direction of said gate electrode.